Amendments to the Specification:

Please amend the paragraph extending from page 21, line 1 through page 21, line 4, to the following:

Then, the variable K is judged whether greater than 3 (K>3) in step S16. If the variable K is not greater than 3 (NO is step S16), the steps [[S4]] S14 to [[S6]] S16 are repeated. If the variable K is greater than 3 (YES in step S16), the fourth sequence #3 is finished in step S17.

Please amend the paragraph extending from page 25, line 28 through page 26, line 3, to the following:

On receipt of the sequence start signal, each of the first to fourth unit modules [[#0]] 11 to [[#3]] 14 carries out the basic processes in each of the sequences #0 to #3. In the embodiment, the first unit module 11 carries out the basic process for the first input buffer #0 in the sequence #0. At this stage, any output ports are not occupied by the input buffers in the sequences #0 to #3.

Please amend the paragraph extending from page 26, line 4 through page 26, line 6, to the following:

In the embodiment, it is assumed that the first module [[#0] 11 gives an allowance to transmit a packet through an output port #1, to the first input buffer #0.